Driving device for scanning single-chip integrated luminous diode array and method thereof

Application Number	97113429	Application Date	1997.05.22
Publication Number	1185686	Publication Date	1998.06.24
Priority Information	US6520751996/5/23		
International Classification	H01L27/00;H03K19/177		
Applicant(s) Name	Motorola Co.		
Address			
Inventor(s) Name	Huang Rongting;Feir Light;Erick D. Joserv		
Patent Agency Code	11038	Patent Agent	yu jing

AbstractA matrix including a plurality of light emitting devices organized into a plurality of rows of first contacts and columns of second contacts. Row/column decoding switches each coupled to a number of individual rows/columns and to a number of row/column address lines for selecting an addressed one of the number of individual rows/columns, and to an individual row/column data lead for selecting a row/column decoding switch. The matrix and row and column switches are integrated onto a common substrate. A programmable voltage source is coupled to the column decoding switches by the column data leads and a programmable current sink is coupled to the row decoding switches by the row data leads.

Application: 97113429

Be used for scanning the driving mechanism and method for of the integrated light emitting-diode array of monolithic

The invention generally relates to the display unit, and relates to a new face driving mechanism that is used for the operation display ware.

More specifically, the invention relates to light emitting device (LED) array, and more precisely relate to the monolithic driving mechanism that integrates mutually with a LED array.

The matrix addressing technique is well-known in the prior art, and has been applied to control various types of displays such as light emitting diode display, liquid crystal device (LCD) display and field launcher spare (FED) display. The matrix addressing scheme becomes the capable and row of a plurality of with emission of light unit or pixel tissue usually, and each pixel lies in delegation and one 's nodical department. Shine the pixel, thereby just need activation crossing line and row provide the closed path route including the pixel that will shine.

Be used for the circuit of the LED matrix display ware of line that the drive has a plurality of pixels and row, include: one have the some the memory of width, wherein this figure equals the figure of pixel; One is listed as the output, be used for the parallel-by-bit of this figure export and be listed as the matrix display ware that the output links to each other; And, one with this memory with be listed as going that the output links to each other and select and the driving circuit, be arranged in selecting the storage complete delegation's figure place of this memory according to and will this complete delegation position provide and be listed as the output.Any one kind of electronic memory that market obtained for example can be followed to the memory that is arranged in the driving circuit, including but not limited to ROM, PROM, EPROM, EEPROM, RAM and so on.

The pictorial information is that the number of pass offers LED driving circuit memory according to the input usually, and with the help of address offering the address in end and by the storage at a preposition.The data of storage latch / row driver and by being offered the LED display at every turn wholely capable through one.Each of the data of each row in this bank all obtains the access and is transmitted the latch cicuit in the memory.These existing data are provided the row driver in order to drive each pixel in this bank simultaneously afterwards.Simultaneously, the new data of delegation when receiving a pulse from a clock, are all selected in proper order to a shift register.The capable actuator disk that receives the line driver of pixel new selected like this, thus by latch / data that the row driver provided the same pixel make the pixel send the light of demand.

There are two kinds to be used for activating appropriate line and with the basic skills of data transfer to appropriate row. A method adopts the decoder, and another kind of method adopts the shift register. To the decoder method, each is gone or row obtain other addressing of branch. It is that those skilled in the art are well-known to loop through the required circuit in these addresses, therefore is not included here in order to simplify the description.

The shift register utilized in the matrix display ware usually not need to go with this facts of arbitrary access of row, they only need obtain addressing in proper order. The advantage of shift register method lies in that it only needs the clock pulses to start a new capable sequence.

What still should pay attention to is that LED matrix display ware can have simple monochromatic configuration, the display that utilizes monochromatic grey level or color monitor.To simple monochrome display, each pixel only needs unit numeral signal, does not turn-off because the pixel is not the switch-on.To the display that adopts monochromatic grey level, need analog signal or long number signal.For example grey level of 16 grades needs the digital signal of quadbit.Each pixel needs at least three emission of light unit usually in the panchromatic demonstration, and each unit is arranged in primary colours (red, green and blue) one kind, and still needs the appropriate light quantity of grey-scale signal system in order to realize every kind of colour.

Usually, in monochromatic escope (black and white), each pixel contains drive that individualistic light emitting device - it must be within the specific limits and switches on (in vain) totally and turn-off the tonal range (grey level) between (deceiving) totally in order realizing. In order to obtain good grey level, the data driver must convey the analog voltage of accuracy each pixel usually. Yet the simulation driving circuit is very dear, and owing to must have hundreds of numbers according to driver (each go light emitting device one), therefore they have constituted the meat and potatoes of display cost.

Further, in the full-color display, each pixel contains at least three light emitting device - its each and all produces different colour (for example red, green and blue) and its each all obtains drive (a common delegation) in order to realize that this specific colour is switching on entirely and the scope of complete shut-down between absolutely in certain range of value(s).Consequently, the figure of the simulation driver that the full-color display contained will many twices, thereby make the manufacturing expense of display increase at least twice.In addition, extra simulation driver needs additional space and power, and this can become the problem in the pocket electronic installation such as BP, honeycomb and conventional phone, radio, database and so on.

As stated, row and the line of LED matrix need or be gone for each row and set up the driver and set up extra latch cicuit for the row driver. This kind of configuration depends on a large amount of I/O terminal counts very much, and the circuit becomes complicated and is not convenient for miniaturizedly.

Display that the messenger has a large amount of emission of light units or a pixel be suitable for pocket application another mainly consider, be the consumption of power.This is the consideration about emission of light unit in the display and drive electronic circuit.In typical case's matrix addressable display, data by the serial input with latch in the circuit of drive emission of light unit.The time that common delegation's (or Lie) is shone is the sub-fraction that the display obtained the time of scanning at every turn.Because high scan rate and a large amount of related pixel figures, therefore with the data immigration with shift out the memory and involve

high clock rate.Need high scan rate and high clock rate, led to the fact excessive dynamic power consumption.

It is very popular in pocket electronics and the communication device field especially in the electronics field, because can send almost any place to a large amount of data and image very rapidly to utilize the display of two-dimensional array or matrix pixel (its each all contain one or a plurality of light emitting device). The problem relevant with these matrixes is that the light emitting device of each line (or Lie) in the matrix must carry out addressing and drive respectively by video or data driver.

Consequently, if the color monitor of display - is especially made at can be enough simpler data driver and I/O terminal still less with still less, will favorable,.

A purpose of the invention provides the new face improvement driven light emitting device matrix that adopts the digital data driver.

Another purpose of the invention is the novel and improvement driven matrix that provides the light emitting device of the less data driver of adoption.

Another purpose of the invention provides the consumed power than prior art display little a lot of matrix display ware and driving circuit of equal value.

Another purpose of the invention is the improvement of separating the code switch that provides LED monolithic matrix.

Another purpose of the invention provides more cheap, the littleer and easier LED display of making.

Another purpose of the invention, be provide a LED display - it will be arranged in row with go to select separate the code switch integration at the integrated array of a monolithic.

Another purpose of the invention provides a LED display, and it has row that are arranged in the LED matrix and the I/O terminal that reduces that the line was selected and counts.

Say briefly that the anticipated purpose according to its best embodiment in order to realize the invention provides a matrix, it includes a plurality of light emitting devices, and a plurality of row that these light emitting devices are formed a plurality of line of compriseing first contact and comprise the second contact. OK / separate the code switch each all with a plurality of solitary line / with a plurality of line / column address line phase coupling with select the solitary line of this a plurality of / in receive of addressing, and with solitary a line / column number according to the lead wire phase coupling in order to select a line / separate code switch.

In best embodiment, matrix and line with be listed as the switch by integrated to the public basement. In addition, code switch phase coupling is separated according to the lead wire with row through the column number in programmable voltage source, and electric current able to programme is subside (current sink) and is separated code switch phase coupling according to the lead wire with going through the line number.

Following following combination figure and elaborating what the best embodiment of the invention was gone on, much more aforementioned and further and the more concrete purpose and the advantage of the invention to those skilled in the art, will become obvious. In the figure:

Fig. 1 simplifies the block diagram, and it has shown the light emitting-diode array that has a driving circuit according to the invention;

The block diagram is simplified to Fig. 2, has shown that a plurality of LED array row separate the code switch;

Fig. 3 has shown that LED array row that Fig. 2 shows separate the truth table of code switch;

Fig. 4 has shown the capable truth table of separating the code switch of LED array;

Fig. 5 is the sketch map, has shown in the block diagram of Fig. 2 that odd one of the a plurality of row that show in separating the code switch is listed as the switching circuit of decoding;

Fig. 6 is the sketch map, has shown a capable switching circuit of decoding of LED array;

Fig. 7 is the sketch map, has shown monolithic light emitting device (LED) the array that has the driving circuit of Fig. 1;

Fig. 8 is the cross-sectional view of simplifying, has shown to be used for row or to go an embodiment of separating the epitaxial structure of code switch; Just

Fig. 9 is the cross-sectional view of simplifying, has shown to be used for row or to go another embodiment of separating the epitaxial structure of code switch.

It has expressed the parts that correspond to see figure - wherein the same reference numeral now in whole pictures; At first see Fig. 1, wherein shown a LED (LED) array integrated circuit 10. Integrated circuit 10 includes by 240 arrays 11 of taking advantage of the appointed pixel of 144 components that each pixel all has being electrically connected of sole row and line. What should understand certainly is, integrated circuit 10 be be used for this description the purpose and in fact can be including any different kinds of array and special row and line and/or different kinds of devices including different figures.

Like demonstration in this embodiment of the invention, a plurality of row are separated code switch 12 and are included that 60 are listed as data signal, C0 to C59. Input signal C0 is appointed as the data signal to C59, and two couples of complemental input signal A_0, A_0, A_1With A_1Be appointed as the addressing signal. Each row is separated code switch 12 and is all shown have input signal A for adding on it_0, A_0, A_1With A_1, and C0 to one of C59.What should understand is, has adopted two signals and their complement code at this, because general individualistic circuit can produce various signals and their complement code, thereby has further saved circuit and chip area.12 phase couplings of code switch are separated with each row to

four of array 11 solitary (promptly respectively and detached) row 13, thus make that a plurality of row separate that code switch 12 can addressing array 11 60 take advantage of 4 240 row 13 altogether promptly.The proposition that code switch 12 was separated to row is in order to be used for with separating the integrated LED array of code switch monolithic, with the I/O count that reduces the chip simultaneously.All row that are used for the column scan separate code switch 12 all the coupling have public address wire A_0, A_0, A_1With A_1Its result, the I/O count that code switch 12 has reduced widely and has shown the pass is separated to the row of proposition. The drive be listed as the unit of circuit 13 the figure reduce to provide these improve, more particularly to reducing of the power consumption of the figure at I/O terminal and array. The device of the addressing row 13 of array 11 is general as follows:

The column selection is selected

If C_0= 1 be 0 with C1 to C59, thereby selects 0,2,4 or 6; And

If C_0= 0, C_1= 1 be 0 with C2 to C59, thereby selects 1,3,5 or 7; And

Through providing high signal by A_0, A_0, A_1Or A_1The difference formed right, and select specific row 1,3,5 or 7.

Set for C0 and be 0, C2=1 with C1, and C3 is 0 to C59, thus selection 8,10,12 or 14 and so on.

Can see now, with the help of to data input pin C0 to C59's activation and to address wire A_0, A_0, A_1With A_1The activation, can keep this kind of sequence to the selection of the row 13 of four separations. Row are separated code switch 12 and are had such characteristic, and this characteristic provides the means that scan in proper order and has reduced the power consumption of array through the figure that reduces chip I/O count.

Shown still in Fig. 1 that a plurality of line separate code switch 15 - its each and all have the a plurality of data-in line R rather than the phase coupling$_0$To R_{35}A solitary data line of (be arranged in in this embodiment 36 line separate code switch 15) altogether. Four solitary (separately just independent promptly) line 14 of array 11 are gone with each and are separated 15 phase couplings of code switch. Each line is separated code switch 15 and is all received the independent data signal R rather than the coupling$_0$To R_{35}And row address line B_0, B_0, B_1With B_1The activation. The effect of the addressing line 14 of array 11 is general as follows:

Go and select

Set for R_0= 1 and R_1To R_{35}For 0, thereby select to go 0,2,4 or 6; Just

Set for R_0= 0 and R_1= 1 and R_2To R_{35}For 0, thereby select to go 1,3,5 or 7; And through providing high signal by B_0, B_0, B_1Or B_1The difference formed to last, and select specific line 1,3,5 or 7.

Set for R_0With R_1= 0, R_2= 1, and R_3To R_{35}For 0, thereby select line 8,10,12 or 14 and so on.

A power able to programme (seeing Fig. 5) is included in the silicon driver IC and as an input to being listed as decoding circuit 12 and obtain connecting.In addition, electric current able to programme is subside circuit (seeing Fig. 6) and is included in this silicon driver IC and as coming from the output of line driver 15 and obtaining connecting.Subside with the help of this power able to programme and electric current able to programme, the figure that is used for separating the device of code switch 12 and 15 can reduce to minimum.All row are separated code switch 12 and are all had public address wire.Its result, row can be scanned in proper order, and its figure that once scans is not more than n/4 (wherein n is the sum of row), depends on the input power that comes from power able to programme.All line are separated code switch 15 and are all had public address wire.Its result, the line can be scanned in proper order, depends on the input power that comes from electric current able to programme and subside, and the figure of the capable decoder 14 that at every turn scans is not more than m/4 (wherein m is the sum of going).The power consumption receives the restriction of silicon driver IC leakage current rather than the MESFET leakage current.11 gained will the hanging down much of LED array of the decoder that its result, power consumption are more traditional than having.本发明因而减小了寻址阵列11的各个LED象素所需的I/O终端的数目，并大大降低了LED集成电路10的功率消耗。

Separating code switch 12 and going that to separate code switch 15 and LED array 11 monolithic in same basement integrated with the help of the low-power row, the power consumption has been reduced greatly. For example, in traditional decoder, above-mentioned 240 take advantage of 11 power that consume of 140LED array to be 11 tiles, and 10 power that consume of LED integrated circuit of the invention are 79 milliwatts. The reduction at I/O terminal from 384 to 140 (in these specific examples), has indicated the great improvement to not separating the integrated LED array of code switch.

See Fig. 2, wherein shown with the form of block diagram that individualistic row separate code switch 12_nThe decoder switch 12_nIncluding a plurality of be listed as decoding circuit 16,17,18 and 19 - they obtain the correct connection with in response to appropriate addressing signal a signal output to the row of LED array 11 0 to the row 3 in. It is relevant with this demonstration, shown in a Fig. 3 truth table 30, it will be quoted when description Fig. 2. Truth table 30 has shown the signal level of each address wire, A promptly$_0$, A_0, A_1With A_1- they are expressed with " 1 " or " 0 ", and code switch 12 is separated to row_nThe high data signal C who provides by power able to $programme_n$Select.

See truth table 30, that should pay attention to is A_0With A_0Complemental signal, and A_1With A_1Complemental signal, therefore when one of a centering being in the logic high, then another is in the logic low. First line 31 has shown selects to be listed as 16 required logical signals in the circuit, pays attention to input line C_nBe in the logic high, A_0With A_1Be in logic low and A_0With A_1Be in the logic high. It is capable 32 to see second in the truth table 30, and it has shown selects to be listed as 17 required logical signals in the circuit, input line C_nStill, be in the logic high, and A_0With A_1Be in logic low and A_0With A_1Be in the logic high. In the third of truth table 30 capable

33 (this bank shown select to be listed as 18 required logical signals in the circuit), input line C_nStill, be in the logic high, and A_0和A_1Be in the logic high, and A_0With A_1Be in the logic low. It is last, in the fourth of truth table 30 capable 34 (it shown select to be listed as 19 required logical signals in the circuit), input line C_nStill, be in the logic high, and A_0With A_1Be in logic high and A_0With A_1Be in the logic low. Consequently, through adding the logic high signal to relevant data input pin C_nOn, just can select any row to separate code switch 12_n, and through utilizing address signal A_0, A_0, A_1With A_1Suitable combination, can select in the row with selected decoder switch 12_nThe any row that link to each other.

Fig. 4 has shown and has been used for going separating code switch 15_nSelection logic truth table 40, it selects similarly with the column selection of truth table 30. Through adding the logic high signal to relevant data input line R_nOn, can select specific line to separate code switch 15_nCode switch 15 is separated to line $selected_n$In, the selection of the delegation in the four lines is with the help of address wire B_0, B_0, B_1With B_1Go on. Output R_0With the help of current sink ware able to programme and subside mutually with an electric current and be electrically connected, and 1 in the logical circuit has been appointed when being connected. As address signal input B_0When being in high level (the quilt is appointed as 1 in truth table 40), the change that comes from the input of address wire confirmed with decoder switch 15_nLink to each other which be about to obtain the activation. Like 30 descriptions in the truth table that combine Fig. 3, the four lines 41 to 44 of truth table 40 has shown to be selected and specific decoder switch 15_nThe required logic of selection of the four lines of relevant array 10.

See Fig. 5, wherein an individualistic circuit 50 that is listed as of signal demonstration understanding code switch 122. If with what describe more in detail, each row are separated code switch 12 and are included all that four are listed as circuit 50. It includes two field effect transistors (FET) 52 and 53 of establishing ties between specific row of power able to programme 54 and array 11 to be listed as circuit 50. In this concrete embodiment, power able to programme 54 and conduct data signal C_nSelected row separate the input phase coupling of code switch 12. In this specifically is listed as the circuit, address wire A_0Link to each other with FET52's grid. Appear at address wire A when the logic $high_0$When going up, FET52 is coupled to a second FET53 to 5 volts of current potentials that are provided by power able to programme 54. When addressing signal A0 was in the logic low, FET52 was not coupled to FET53 to these 5 volts of current potentials.

Address wire A1 links to each other with FET53's grid through two level shift diodes 55 and 56, and level shift diode 55 and 56 and address wire A_1Establish ties. 55 and 56 grids to FET53 of level shift diode provide the voltage removal, with the forward bias of grid - drain electrode diode of preventing FET53. With the help of the MESFET circuit, level shift diode 55 and 56 is used for preventing that the MESFET grid from being driven into the forward bias. If shown, field effect transistor 53 is as address wire $A_1$5 volts of current potentials that switch on when being in the high level and will come from FET52 are coupled to the corresponding row (is shown and be terminal 57) of array 11. Address wire A_1On the logic low switching on of FET28 has stoped.

See Fig. 6, a capable circuit 60 has obtained the signal and has shown that four such circuit have constituted a complete line and have separated code switch 15. Go circuit 60 including establish ties the corresponding line of array 11 and electric current subside between 64 two FET62 and 63, and the electric current to subside 64 be that aforesaid able to programme electricity is subside. Here in the concrete embodiment, electricity able to programme subside 64 with as data signal R_nSelected line separate the input phase coupling of code switch 15. As address wire B_0When adding the logic high signal to the grid, FET62 is coupled to FET63 with the corresponding line of array 11. Address wire B_1Must be in the logic high, could activate FET63 and subside 64 circuit to the electric current in order to accomplish. The electric current is subside 64 and is added to data line R when the logic high $signal_n$(it is a terminal to be shown in Fig. 6) last time is by electric coupling to FET63. The electric current is subside 64 and must be electrically connected, so that the electric current can flow through line circuit 60. Walk to the electric current from array 11 corresponding and subside 64 electric conductivity, accomplished activate concrete addressing LED so that its luminous circuit (supposing that at least one is listed as circuit 50 and has obtained the activation).

See Fig. 7, LED array integrated circuit 10 has obtained the signal and has shown.Its some part has been detached.Integrated circuit 10 includes the a plurality of LED in LED matrix 11.As an example, specific LED70's a terminal be electrically connected to that first row separate code switch 12 (in the picture for convenient and surround with the dotted line) first be listed as circuit 50 (being shown alone) in Fig. 5.LED70's second terminal with to go 60 (being shown alone) of a first capable circuit of separating in the code switch 15 (in order convenient and surround) with the dotted line link to each other in Fig. 6, separate indivedual demonstrations that the code switch was separated to code switch and a plurality of line in order regard as to a plurality of row of being used for activating LED array 11 and a plurality of row of line.This picture has shown four LED circuit arrangements of Fig. 2, and code switch 12 is separated through being connected to power able to programme 54 row of addressing and activating four row to one of them row, and corresponding line is separated code switch 15 and is electrically connected to the electric current and subsides 62 through being separated code switch 15 from four line by going of addressing, and has accomplished this circuit.Be listed as circuit 50 circuit or the switch in through power able to programme 54 (by showing for pieces 72), and with data line C_0On power able to programme 54 link to each other, perhaps accomplish to the circuit of powers able to programme 54 with other modes. Likewise, a switch OR circuit in 64 (showing for piece 74) is subside through electric current able to programme to the circuit 60 of going, and with data signal R_0On electric current able to programme subside 64 and link to each other, perhaps accomplish with other modes and subside 64 circuit to the electric current.

What should understand is that power able to programme 54 subsides 64 with electric current able to programme, except the power volume in that any preset time provided is able to programme, can also obtain the programming, in order to pass through data line C_0To C_{58}On the input signal the preset program and at data line R_0To R_{35}On the preset program of input signal automatically sort.

What Fig. 8 was shown is that code switch 82 (showing for individualistic FET) and LED array 83 (showing for individualistic LED) the epitaxial structure 80 of

monolithic integration in same basement are separated to the low-power.LED array 83 includes the a plurality of doping and epitaxial layers that do not mix that form in proper order in semi-insulating GaAs basement 84.If shown, AIGaInP layer that these epitaxial layers are n+-GaAs layer 85, n-InGap layer 86, n-AlInP layer 87, do not mix 88, the AlInP layer of not mixing 89,90, about 200 thick P-InGaP layers 91 and about 500 thick not doping GaAs layer 92 on the P-AlInP layer, with form with the 82 LED arrays 83 that integrate mutually on the corresponding switch.Insulating and the plug-in strip that sets up of the still promising pixel that shows 94, the plug-in strip 95 that provides for being electrically connected of the lower end to each pixel and for going the plug-in strip 96 that the insulation provided.With the help of contact 97 and 98, the metallization that provides each LED to the array 83 in is connected.Switch 82 includes the insulating plug-in strip of device 100, source electrode and drain electrode connection plug-in strip 102 and 104 and is used for the metallization contact 112,113 and 114 of source electrode, grid and drain electrode respectively.On September 26th, 1995 that issue, exercise question for " inserting the manufacturing approach of LED array " and in transferring same assignee's United States Patent (USP) the 5,453,386th number, can find other information of relevant this kind of array.In addition, about the integrated technology, see on January 9th, 1996 that issue, exercise question for " the electricity - optic integrated circuit that has the diode decoder " and transfer same assignee's United States Patent (USP) the 5,483,085th number.

Shown the epitaxial structure 120 of a correction in Fig. 9, it includes separates code switch 122 with the integrated mode of monolithic and LED array 130 are integrated in same basement. The LED array of LED array 130 and Fig. 8 is 83 similar. The switch of separating code switch 122 and Fig. 8 is 82 similar, and just it is being through adding extra epitaxial layer on LED array 130 to FET122 and make from LED130 during the device manufacturing, thereby the diffusion of messenger p alloy is comparatively easy.

Consequently, announced with making the especially method of color monitor of display in more simple and few data driver and I/O terminal still less.Still announce the new face modified light emitting device drive matrix that utilizes the digital data driver, and especially utilized the light emitting device matrix of less data driver.In addition, much little and more cheap, littleer and easier matrix display ware and the driver circuit of making of the corresponding prior art display of used power ratio has still been announced.The invention provides a LED display, it will be arranged in row with go select separate the code switch integration at the integrated array of monolithic, and be used for row in the LED matrix and go the I/O terminal figure of selecting having reduced a lot.What certainly still should understand is, can be only with row or go and decode the switch module and provide LED the display, and other line or row are decoded that switch module (these yes interchangeable) can be connected with normal hardware, the decoding of certain form, shift register and so on are come substitutedly.

Subside with the help of power able to programme and electric current able to programme, the figure that is used for separating the device of code switch can reduce to minimum. The power consumption through the driver leakage current rather than the MESFET leakage current and obtain the restriction. Its result, the power

consumption is than adopting do not take power able to programme to programme gained will the hanging down much of array that the electric current subsides.

All row are separated the code switch and are all had public address wire. Its result, row can be scanned with n/4's mode in proper order, and wherein n is column number once and depends on the input power that comes from the driver. All line are separated the code switch and are all had public address wire. Its as a result the line can be in proper order or obtain scanning with m/4's mode, wherein m is line number once and depends on the state that electric current able to programme subsides. Be used for preventing that the MESFET grid from being driven the level shift diode of forward bias state, the quilt scans in order to provide the on off sequence of decoding on being placed in a CMOS driver.

The invention has reduced the figure at the I/O terminal of activation LED pixel, and has reduced greatly the power consumption of LED integrated circuit. Through separating the low-power code switch and the integration of LED array monolithic in same basement, power has obtained reducing greatly. For example, in traditional decoder, be used for 240 power of taking advantage of the 140LED array to be 11 tiles, and only 36 milliwatts of separating code switch LED array of the invention. 384 to 140 reduction - follows at I/O terminal have improved the LED array widely, and need not integrate and separate the code switch.

Be conspicuous to the various corrections and the change of the embodiment selected for the purpose of explanation here to those skilled in the art. For example, the integrated circuit can be made with any convenient Semiconductor Materials system or any convenient organic system. In addition, LED array and switch can be made with various modes, and still can carry out said function. In addition, can adopt the light emitting device of various differences, and these devices can be made with the step of revising to a certain extent and/or exchanging.

Abovely just describe with the mode of giving an example. Under the prerequisite of the scope that does not break away from the invention of the claims, those skilled in the art can make various other corrections and change.

It is above with clear and definite and the invention and best embodiment are fully described and announced to simple and clear mode, thus make those skilled in the art can understand and implement the invention and best embodiment.

CLAIMS

1. light emitting device driving mechanism and matrix characterized in:A matrix, including a plurality of light emitting devices, each light emitting device all has first contact and second contact, and it is capable that a plurality of first contacts are formed to first contact, and a plurality of second contact row are formed to the second contact;The code switch is separated to a plurality of line, and each is gone and separates the electric current that the code switch all has the solitary capable phase coupling of a plurality of in a plurality of line of forming with first contact and bear the weight of the end;A plurality of row address lines, its each all separate each phase coupling in the code switch with a plurality of line, separate one that receives the addressing in the a plurality of independent line in each in the code switch in order to

select to be coupled to a plurality of line;The code switch phase coupling is separated according to lead wire, each relevant line number according to lead wire and each line to a plurality of line numbers, separates the code switch with the line number that convenient activation signal is added to relevant according to line of lead wire selection of last time;The code switch is separated to a plurality of row, and each row is separated the solitary electric current that is listed as the phase coupling of a plurality of that the code switch all has in a plurality of row of forming with the second contact and is born the weight of the end;A plurality of column address lines, its each all be coupled to on a plurality of row separate each in the code switch, of addressing is received in the row alone with the a plurality of of selecting to separate each phase coupling in the code switch with a plurality of row;A plurality of column numbers are according to the lead wire, and each relevant column number all is coupled to on row separate each in the code switch according to the lead wire, and the code switch is separated to row of selection when being offered relevant column number according to the lead wire with convenient activation signal.

2. light emitting device driving mechanism and the matrix according to claim 1, its further characteristic lies in that electrically driven device includes one in organic light emitting device, semiconductor LED and the liquid crystal device.

3. light emitting device driving mechanism and the matrix according to claim 1, its further characteristic lie in that a plurality of row separate in the code switch each and all include the first transistor that has the electric current and bear the weight of electrode and control electrode, and wherein this electric current bears the weight of the electrode and has formed row and separate first and second electric currents of code switch and bear the weight of the end.

4. light emitting device driving mechanism and the matrix according to claim 3, its further characteristic lie in that a plurality of row separate in the code switch each and all further include a second transistor, and this second transistor has and bears the weight of the first electric current that the end links to each other with the second electric current of the first transistor and bear the weight of the electrode; A second electric current bears the weight of the end; A plurality of diodes; With a control electrode.

5. light emitting device driving mechanism and the matrix according to claim 4, its further characteristic lie in a plurality of row separate in the code switch each all include in a plurality of column address lines with first and a plurality of column address line of the control electrode phase coupling of the first transistor in with the second of the control electrode phase coupling of second transistor.

6. light emitting device driving mechanism and the matrix according to claim 1, its further characteristic lie in that a plurality of line separate in the code switch each and all include the first transistor that has the electric current and bear the weight of electrode and control electrode, and wherein this electric current bears the weight of the electrode and has formed and go first and second electric currents of separating the code switch and bear the weight of the end.

7. light emitting device driving mechanism and the matrix according to claim 6, its further characteristic lie in separating the code switch by a plurality of line each all

further include a second transistor, and this second transistor has and bears the weight of with the second electric current of the first transistor that the first electric current that the end links to each other bears the weight of the electrode, a second electric current bears the weight of end, a plurality of diode and a control electrode.

8. light emitting device driving mechanism and the matrix according to claim 7, its further characteristic lie in a plurality of line separate the code switch each all include in a plurality of row address lines with article one of the control electrode phase coupling of the first transistor and a plurality of row address line in with the second of the control electrode coupling of second transistor.

9. light emitting device driving mechanism and the matrix according to claim 1, its further characteristic lie in that a programmable voltage source and a plurality of column numbers provide electric power and have an electric current able to programme to subside and provide the electric current and subside in order to be used for separating code switch and relevant line to selected line according to the lead wire phase coupling with a plurality of line numbers in order to be used for separating code switch and relevant row to selected row according to the lead wire phase coupling.

10. be used for the method of addressing light emitting device matrix, characterized in following step:Provide a matrix, this matrix includes a plurality of light emitting devices, and each light emitting device all has first contact and second contact, and the capable and a plurality of second contact row of second contact component of a plurality of first contacts are formed to these first contacts;Provide a plurality of line and separate the code switch, each all with R_0To R_nA phase coupling in the lead wire is offered R with convenient activation $signal_0$To R_nThe code switch is separated to the line of one of lead wire when lasting selection coupling, a plurality of line separate in the code switch each further with at least four the capable phase couplings of first contact (wherein n is greater than any integer of 0);Provide at least B_0, B_0, B_1With B_1Row address line, wherein B_0With B_0Be the complementary signal $just_B1$ and B_1Be the complementary signal, each all is coupled to a plurality of line separates in each in the code switch in order to select separating that receives the addressing in four solitary line of each phase coupling in the code switch with a plurality of line;Provide a plurality of row and separate the code switch, its each all with C_0To C_mA phase coupling in the lead wire is offered C with convenient activation $signal_0$To C_mThe code switch is separated to the row of selecting to obtain the coupling during in the lead wire one, a plurality of row separate in the code switch each all be listed as phase coupling (wherein m is greater than any integer of 0) with at least four second contacts further;Provide at least A_0, A_0, A_1With A_1Column address line, wherein A_0With A_0Complementary signal and A_1With A_1Be the complementary signal, its each all separate each phase coupling in the code switch with a plurality of row, be arranged in selecting separating one that receives the addressing in four row of each phase coupling of code switch with a plurality of row; AndThrough selecting R_0To R_nOne and B in the lead $wire_0$, B_0, B_1With B_1The combination and the selection C of row address $line_0$To C_mOne and A in the lead $wire_0$, A_0, A_1With A_1The combination of column address line carries out the addressing to the concrete light emitting device of matrix.

[19]中华人民共和国专利局

[51]Int.Cl[6]
H03K 19/177
H01L 27/00

[12] 发明专利申请公开说明书

[21] 申请号 97113429.4

[43]公开日 1998 年 6 月 24 日

[11] 公开号 CN 1185686A

[22]申请日 97.5.22

[30]优先权

[32]96.5.23 [33]US[31]652075

[71]申请人 摩托罗拉公司

地址 美国伊利诺斯

[72]发明人 黄荣庭 非尔·莱特
埃里克·D·约瑟夫

[74]专利代理机构 中国国际贸易促进委员会专利商标事务所

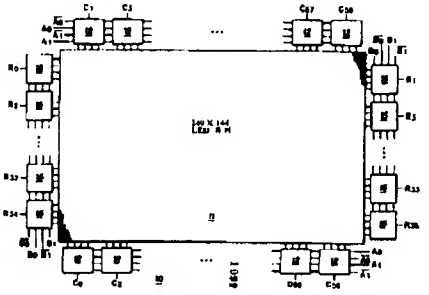
代理人 于 静

权利要求书 3 页 说明书 11 页 附图页数 5 页

[54]发明名称 用于扫描单片集成发光二极管阵列的驱动装置和方法

[57]摘要

一种矩阵包括多个发光器件，这些器件组成了多个第一触头行和第二触头列。行／列解码开关每一个都与若干单独的行／列和若干行／列地址线相耦合，以选择若干单独的行／列中受到寻址的一个，并与单独的行／列数据引线相耦合以选择一个行／列解码开关。该矩阵和行和列开关被集成到一个公共基底上。一个可编程电压源通过列数据引线而与该列解码开关耦合，且一个可编程电流陷落通过行数据引线而与该行解码开关耦合。



权 利 要 求 书

1. 一种发光器件驱动装置和矩阵，其特征在于:

一个矩阵，包括多个发光器件，每一个发光器件都具有第一触头和第二触头，第一触头组成多个第一触头行，且第二触头组成多个第二触头列;

多个行解码开关，每一个行解码开关都具有与第一触头组成的多个行中的若干个单独的行相耦合的电流承载端;

多个行地址线，其每一个都与多个行解码开关中的每一个相耦合，以选择耦合到多个行解码开关中的每一个上的若干单独行中受到寻址的一个;

多个行数据引线，每一个有关的行数据引线与每一个行解码开关相耦合，以便当激活信号被加到有关的行数据引线上时选择一个行解码开关;

多个列解码开关，每一个列解码开关都具有与第二触头组成的多个列中的若干个单独的列相耦合的电流承载端;

多个列地址线，其每一个都耦合到多个列解码开关中的每一个上，以选择与多个列解码开关中的每一个相耦合的若干个单独列中受到寻址的一个;

多个列数据引线，每一个相关的列数据引线都耦合到列解码开关中的每一个上，以便当激活信号被提供给有关的列数据引线时选择一个列解码开关。

2. 根据权利要求 1 所述的发光器件驱动装置和矩阵，其进一步的特征在于电流驱动装置包括有机发光器件、半导体发光二极管和液晶器件中的一个。

3. 根据权利要求 1 所述的发光器件驱动装置和矩阵，其进一步的特征在于多个列解码开关中的每一个都包括带有电流承载电极和控制电极的第一晶体管，其中该电流承载电极形成了列解码开关的第一和第二电流承载端。

4. 根据权利要求 3 所述的发光器件驱动装置和矩阵，其进一步的特征

在于多个列解码开关中的每一个都进一步包括一个第二晶体管，该第二晶体管带有与第一晶体管的第二电流承载端相连的第一电流承载电极；一个第二电流承载端；多个二极管；和一个控制电极。

5. 根据权利要求 4 所述的发光器件驱动装置和矩阵，其进一步的特征在于多个列解码开关中的每一个都包括多个列地址线中与第一晶体管的控制电极相耦合的第一个，和多个列地址线中与第二晶体管的控制电极相耦合的第二个。

6. 根据权利要求 1 所述的发光器件驱动装置和矩阵，其进一步的特征在于多个行解码开关中的每一个都包括带有电流承载电极和控制电极的第一晶体管，其中该电流承载电极形成了行解码开关的第一和第二电流承载端。

7. 根据权利要求 6 所述的发光器件驱动装置和矩阵，其进一步的特征在于多个行解码开关每一个都进一步包括一个第二晶体管，该第二晶体管带有与第一晶体管的第二电流承载端相连的第一电流承载电极、一个第二电流承载端、多个二极管和一个控制电极。

8. 根据权利要求 7 所述的发光器件驱动装置和矩阵，其进一步的特征在于多个行解码开关每一个都包括多个行地址线中与第一晶体管的控制电极相耦合的第一条，和多个行地址线中与第二晶体管的控制电极耦合的第二条。

9. 根据权利要求 1 所述的发光器件驱动装置和矩阵，其进一步的特征在于有一个可编程电压源与多个列数据引线相耦合以用于向选定的列解码开关和有关的列提供电力，和有一个可编程电流陷落与多个行数据引线相耦合以用于向选定的行解码开关和有关的行提供电流陷落。

10. 用于寻址发光器件矩阵的方法，其特征在于以下步骤：

提供 一个矩阵，该矩阵包括多个发光器件，而每一个发光器件都具有第一触头和第二触头，这些第一触头组成多个第一触头行且第二触头组成多个第二触头列；

提供多个行解码开关，每一个都与 R_0 至 R_n 引线中的一条相耦合以便当激活信号被提供给 R_0 至 R_n 引线之一上时选择耦合的行解码开关，多个行解

码开关中的每一个进一步地与至少四个第一触头行相耦合（其中 n 是大于 0 的任何整数）；

提供至少 B_0、$\overline{B_0}$、B_1和$\overline{B_1}$行地址线，其中 B_0和$\overline{B_0}$是互补信号且 B_1和$\overline{B_1}$是互补信号，每一个都耦合到多个行解码开关中的每一个上以选择与多个行解码开关中的每一个相耦合的四个单独的行中受到寻址的一个；

提供多个列解码开关，其每一个都与 C_0至 C_n引线中的一条相耦合，以便当激活信号被提供给 C_0至 C_n引线中的一条时选择得到耦合的列解码开关，多个列解码开关中的每一个都进一步地与至少四个第二触头列相耦合（其中 m 是大于 0 的任何整数）；

提供至少 A_0，$\overline{A_0}$，A_1和$\overline{A_1}$列地址线，其中 A_0和$\overline{A_0}$是互补信号且 A_1和$\overline{A_1}$是互补信号，其每一个都与多个列解码开关中的每一个相耦合，用于选择与多个列解码开关中的每一个相耦合的四个列中受到寻址的一个；以及

通过选择 R_0至 R_n引线中的一个以及 B_0，$\overline{B_0}$，B_1和$\overline{B_1}$行地址线的组合以及选择 C_0至 C_n引线中的一个与 A_0，$\overline{A_0}$，A_1和$\overline{A_1}$列地址线的组合，来对矩阵的具体发光器件进行寻址。

说　　明　　书

用于扫描单片集成发光二极管阵列的驱动装置和方法

本发明一般地涉及显示装置，且更具体地说是涉及一种用于操作显示器的新颖的驱动装置。

更具体地说，本发明涉及发光器件（LED）阵列，且更准确地说是涉及与一个LED阵列相集成的单片驱动装置。

矩阵寻址技术是现有技术中众所周知的，并已经被应用于控制各种类型的显示器—诸如发光二极管显示器，液晶器件（LCD）显示器、以及场致发射器件（FED）显示器。矩阵寻址方案通常将光发射单元或象素组织成若干个行和列，而每一个象素位于一行和一列的交点处。对象素进行照射，就需要激活相交的行和列从而提供包括所要照射的象素的闭合电流通路。

用于驱动带有多个象素的行和列的LED矩阵显示器的电路，包括：一个具有一定数目的位的宽度的存储器，其中该位的数目等于象素的数目；一个列输出端，用于把该数目的位并行地输出到与列输出端相连的矩阵显示器；以及，一个与该存储器和列输出端相连的行选择和驱动电路，用于选择存储在该存储器中的完整的一行位数据并将该完整的一行位提供到列输出端。用于驱动电路的存储器是例如可以从市场上获得的电子存储器中的任何一种，包括但不限于ROM、PROM、EPROM、EEPROM、RAM等等。

图象信息通常是通过数据输入端而提供给LED驱动电路存储器的，并借助提供给地址输入端的一个地址而被存储在一个预定的位置。存储的数据通过一个锁存/列驱动器而被每次一整行地提供给LED显示器。该行中的每一列的数据的每一位，都在存储器中得到存取并被传递到锁存电路。该现行数据随后被提供到列驱动器以同时驱动该行中的每一个象素。同时，一个移位寄存器，每当从一个时钟接收到一个脉冲时，都依次选择一行新的数据。这样新选定的象素行受到行驱动器的致动，从而由锁存/列驱动器提供到相同的象素的数据使得象素发出所需量的光。

有两种用于激活适当的行和将数据传送到适当的列的基本方法。一种方法采用解码器，而另一种方法采用移位寄存器。对于解码器方法，每一个行或列得到分别的寻址。依次通过这些地址所需的电路是本领域的技术人员众所周知的，因而为了简化描述而没有被包括在此。

移位寄存器利用了在矩阵显示器中通常不需要对行和列的随机存取这一事实，它们只需要得到依次寻址。移位寄存器方法的优点在于它只需要时钟脉冲来启动一个新的行序列。

还应该注意的是，LED 矩阵显示器可以具有简单的单色配置、利用单色灰度的显示器或彩色显示器。对于简单的单色显示器，每一个象素只需要一个位数字信号，因为象素不是接通就是关断。对于采用单色灰度的显示器，需要模拟信号或多位数字信号。例如一个十六级的灰度需要四位的数字信号。全色显示中每一个象素通常需要至少三个光发射单元，每一个单元用于基色（红、绿和蓝）中的一种，且还需要一种灰度信号系统以实现每种颜色的适当的光量。

通常，在单色型显示器（黑白）中，每一个象素包含单个的发光器件—它必须在一定范围内的驱动以实现完全导通（白）和完全关断（黑）之间的灰度范围（灰度级）。为了获得良好的灰度，数据驱动器通常必须能够将准确的模拟电压传送到各个象素。然而，模拟驱动电路是非常昂贵的，且由于必须有数百个数据驱动器（每一行发光器件一个），因而它们构成了显示器成本的主要部分。

进一步地，在全色显示器中，每一个象素包含至少三个发光器件—其每一个都产生不同的颜色（例如红、绿和蓝）且其每一个都在一定值的范围中得到驱动（通常一次一行）以实现该特定颜色在全导通和全关断之间的一个范围。因此，全色显示器所包含的模拟驱动器的数目要多两倍，从而使显示器的制造费用增大了至少两倍。另外，额外的模拟驱动器需要额外的空间和功率，而这在诸如寻呼机、蜂窝和常规电话、收音机、数据库等等的袖珍电子装置中将会成为问题。

如上所述，LED 矩阵的列和行需要为每一列或行设置驱动器并为列驱动器设置额外的锁存电路。这种配置非常地依赖于大量的 I/O 终端计数，

且电路变得复杂且不便于小型化。

使具有大量光发射单元或象素的显示器适合于袖珍应用的另一个主要考虑，是功率的消耗。这是关于显示器中的光发射单元以及驱动电子电路的考虑。在典型的矩阵可寻址显示器中，数据被串行输入和锁存在驱动光发射单元的电路中。通常一行（或列）得到照射的时间只是显示器每次得到扫描的时间的一小部分。由于高的扫描速率和大量的所涉及的象素数目，因而将数据移入和移出存储器涉及到高的时钟速率。需要高扫描速率和高时钟速率，造成了过度的动态功率消耗。

利用两维阵列或矩阵象素（其每一个都包含一或多个发光器件）的显示器，在电子领域特别是袖珍电子和通信装置领域中是非常流行的，因为能够非常迅速地把大量的数据和图象发送到几乎任何地方。与这些矩阵有关的一个问题，是矩阵中每一行（或列）的发光器件必须由视频或数据驱动器分别地进行寻址和驱动。

因此，如果能够用更简单和更少的数据驱动器和更少的 I/O 终端来制造显示器—特别是彩色显示器，将是有利的。

本发明的一个目的，是提供采用数字数据驱动器的新颖的改进驱动的发光器件矩阵。

本发明的另一个目的，是提供采用较少数据驱动器的发光器件的新颖和改进驱动 的矩阵。

本发明的再一个目的，是提供消耗功率比等价的现有技术显示器小很多的矩阵显示器和驱动电路。

本发明的再一个目的，是提供对 LED 单片矩阵的解码开关的改进。

本发明的再一个目的，是提供更便宜、更小且更容易制造的 LED 显示器。

本发明的再一个目的，是提供一种 LED 显示器—它将用于列和行选择的解码开关集成在一个单片集成阵列中。

本发明的再一个目的，是提供一种 LED 显示器，它带有用于 LED 矩阵中的列和行选择的减小的 I/O 终端计数。

简要地说，为了实现本发明的根据其最佳实施例的预期目的，提供了

一种矩阵，它包括多个发光器件，而这些发光器件被组成由第一触头组成的多个行和由第二触头组成的多个列。行/列解码开关每一个都与若干单独的行/列和若干行/列地址线相耦合以选择该若干个单独的行/列中受到寻址的一个，并与一个单独的行/列数据引线相耦合以选择一个行/列解码开关。

在最佳实施例中，矩阵和行和列开关被集成到一个公共基底上。另外，一个可编程电压源通过列数据引线而与列解码开关相耦合，且一个可编程电流陷落（current sink）通过行数据引线而与行解码开关相耦合。

从以下结合附图对本发明的最佳实施例所进行的详细描述，本发明的前述和进一步及更多的具体目的和优点，对于本领域的技术人员来说，将变得显而易见。在附图中:

图 1 是简化框图，它显示了根据本发明的带有驱动电路的发光二极管阵列;

图 2 是简化框图，显示了多个 LED 阵列列解码开关;

图 3 显示了图 2 显示的 LED 阵列列解码开关的真值表;

图 4 显示了 LED 阵列行解码开关的真值表;

图 5 是示意图，显示了在图 2 的框图中显示的多个列解码开关中的单个列解码开关电路;

图 6 是示意图，显示了一个 LED 阵列行解码开关电路;

图 7 是示意图，显示了带有图 1 的驱动电路的单片发光器件（LED）阵列;

图 8 是简化的横截面图，显示了用于列或行解码开关的外延结构的一个实施例；且

图 9 是简化的横截面图，显示了用于列或行解码开关的外延结构的另一实施例.

现在参见附图—其中相同的标号在全部图中表示了对应的部件；首先参见图 1，其中显示了一个发光二极管（LED）阵列集成电路 10．集成电路 10 包括由 240 乘 144 个元件指定象素的阵列 11，每一个象素都具有唯一的列和行的电连接。当然应该理解的是，集成电路 10 是用于本说明书的

目的的且实际上可以包括任何不同类型的阵列和特别包括不同数目的列和行和/或不同类型的器件。

如在本发明的该实施例中所显示的，多个 列解码开关 12 包括 60 个列数据信号， C0 至 C59 。输入信号 C0 至 C59 被指定为数据信号， 且两对互补的输入信号 A_0、 $\overline{A_0}$、 A_1和 $\overline{A_1}$ 被指定为寻址信号。 每一个列解码开关 12 都被显示为其上加有输入信号 A_0、 $\overline{A_0}$、 A_1和 $\overline{A_1}$、以及 C0 至 C59 之一。应该理解的是， 在此只采用了两个信号和它们的补码，因为一般单个的电路能够产生各种信号和它们的补码， 从而进一步节省了电路和芯片面积。阵列 11 的四个单独的（即分别而分开的）列 13 与每一个列解码开关 12 相耦合，从而使多个列解码开关 12 能够寻址阵列 11 的 60 乘 4 即总共 240 个列 13 。列解码开关 12 的提出， 是为了用于同解码开关单片集成的 LED 阵列，以同时减小芯片的 I/O 计数。 所有用于列扫描的列解码开关 12 都耦合有公共的地址线 A_0、 $\overline{A_0}$、 A_1和 $\overline{A_1}$。其结果，提出的列解码开关 12 大大地减小了与列有关的 I/O 计数。驱动列电路 13 的单元的数目的减小所提供的这些改进，特别涉及 I/O 终端的数目和阵列的功率消耗的减小。阵列 11 的寻址列 13 的装置一般如下:

列选择

设 C_0 = 1 和 C1 至 C59 为 0，从而选择列 0 、 2 、 4 或 6； 以及

通过把高信号提供到由 A_0、 $\overline{A_0}$、 A_1或 $\overline{A_1}$组成的不同的对（例如 A_0、A_1； A_0、 $\overline{A_1}$； $\overline{A_0}$、 A_1； 或 $\overline{A_0}$、 $\overline{A_1}$ ）而选择具体的列 0 、 2 、 4 或 6 。

设 C_0 = 0， C_1 = 1 和 C2 至 C59 为 0，从而选择列 1 、 3 、 5 或 7； 并

通过把高信号提供到由 A_0、 A_0、 A_1或 A_1组成的不同的对，而选择具体的列 1 、 3 、 5 或 7 。

设定 C0 和 C1 为 0， C2 = 1 ，且 C3 至 C59 为 0 ，从而选择列 8 、 10 、 12 或 14 等等.

现在可以看到，借助对数据输入端 C0 至 C59 的激活以及对地址线 A_0、$\overline{A_0}$、 A_1和 $\overline{A_1}$的激活， 能够对四条分立的列 13 的选择保持这种序列。 列解码开关 12 具有这样的特性， 该特性提供了依次扫描的手段并通过减小芯

片 I/O 计数的数目而减小了阵列的功率消耗。

在图 1 中还显示了多个行解码开关 15 一其每一个都带有与其相耦合的多个输入数据线 R_0 至 R_{35}（在本实施例中用于总共 36 个行解码开关 15）中的一个单独的数据线。阵列 11 的四个单独的（即分开且独立的）行 14 与每一个行解码开关 15 相耦合。每一个行解码开关 15 都受到与其耦合的单独数据信号 R_0 至 R_{35} 以及行地址线 B_0、$\overline{B}_0$、B_1 和 $\overline{B}_1$ 的激活。阵列 11 的寻址行 14 的作用一般如下：

行选择

设定 R_0 = 1 且 R_1 至 R_{35} 为 0，从而选择行 0、2、4 或 6；且

通过把高信号提供到由 B_0，$\overline{B}_0$，B_1，$\overline{B}_1$ 组成的不同的对上（例如 B_0，B_1；B_0，$\overline{B}_1$；$\overline{B}_0$，B_1 或 $\overline{B}_0$，$\overline{B}_1$）而选择具体的行 0、2、4 或 6。

设定 R_0 = 0 和 R_1 = 1 且 R_2 至 R_{35} 为 0，从而选择行 1、3、5 或 7；且通过把高信号提供到由 B_0、$\overline{B}_0$、B_1 或 $\overline{B}_1$ 组成的不同的对上，而选择具体的行 1、3、5 或 7。

设定 R_0 和 R_1 = 0，R_2 = 1，且 R_3 至 R_{35} 为 0，从而选择行 8、10、12 或 14 等等。

一个可编程电源（见图 5）被包括在硅驱动器集成电路中并作为至列解码电路 12 的一个输入端而得到连接。另外，一个可编程电流陷落电路（见图 6）被包括在该硅驱动器集成电路中并作为来自行驱动器 15 的输出端而得到连接。借助该可编程电源和可编程电流陷落，用于解码开关 12 和 15 的器件的数目能够减到最小。所有的列解码开关 12 都具有公共地址线。其结果，列能够得到依次扫描，其一次扫描的数目不大于 n/4（其中 n 是列的总数），取决于来自可编程电源的输入功率。所有的行解码开关 15 都具有公共地址线。其结果，行能够得到依次扫描，取决来自可编程电流陷落的输入功率，每次扫描的行解码器 14 的数目不大于 m/4（其中 m 是行的总数）。功率消耗受到硅驱动器集成电路漏电流而不是 MESFET 漏电流的限制。其结果，功率消耗比带有传统的解码器的 LED 阵列 11 所获得的要低得多。本发明因而减小了寻址阵列 11 的各个 LED 象素所需的 I/O 终端的数目，并大大降低了 LED 集成电路 10 的功率消耗。

借助低功率列解码开关 12 和行解码开关 15 与 LED 阵列 11 在同一基底上的单片集成，功率消耗被大大减小了。例如，在传统的解码器中，上述 240 乘 140 LED 阵列 11 所消耗的功率为 11 瓦，而本发明的 LED 集成电路 10 所消耗的功率为 79 毫瓦。I/O 终端的减少，从 384 至 140（在这个具体的例子中），表明了对没有解码开关集成的 LED 阵列的重大改进。

参见图 2，其中以框图的形式显示了一个单个的列解码开关 12_n。解码器开关 12_n 包括多个列解码电路 16、17、18 和 19 —它们得到适当连接以响应于适当的寻址信号而把一个信号输出到 LED 阵列 11 的列 0 至列 3 中的一个。与该显示有关的，是图 3 中所示的一个真值表 30，它将在描述图 2 时得到引用。真值表 30 显示了各个地址线的信号电平，即 A_0、$\overline{A}_0$、A_1 和 $\overline{A}_1$—它们用“1”或“0”表示，而列解码开关 12_n 由可编程电源提供的高数据信号 C_n 选择。

参见真值表 30，应该注意的是 A_0 和 $\overline{A}_0$ 是互补的信号，且 A_1 和 $\overline{A}_1$ 是互补的信号，因而当一对中的一个处于逻辑高电平时，则另一个处于逻辑低电平。第一行 31 显示了选择列电路 16 所需的逻辑信号，注意输入线 C_n 处于逻辑高电平，A_0 和 A_1 处于逻辑低电平且 $\overline{A}_0$ 和 $\overline{A}_1$ 处于逻辑高电平。参见真值表 30 中的第二行 32，它显示了选择列电路 17 所需的逻辑信号，输入线 C_n 仍然处于逻辑高电平，而 A_0 和 $\overline{A}_1$ 处于逻辑低电平且 $\overline{A}_0$ 和 A_1 处于逻辑高电平。在真值表 30 的第三行 33（该行显示了选择列电路 18 所需的逻辑信号）中，输入线 C_n 仍然处于逻辑高电平，而 A_0 和 $\overline{A}_1$ 处于逻辑高电平，且 $\overline{A}_0$ 和 A_1 处于逻辑低电平。最后，在真值表 30 的第四行 34（它显示了选择列电路 19 所需的逻辑信号）中，输入线 C_n 仍然处于逻辑高电平，而 A_0 和 A_1 处于逻辑高电平且 $\overline{A}_0$ 和 $\overline{A}_1$ 处于逻辑低电平。因此，通过把逻辑高电平信号加到有关的数据输入端 C_n 上，就可以选择任何列解码开关 12_n，且通过利用地址信号 A_0、$\overline{A}_0$、A_1 和 $\overline{A}_1$ 的适当组合，可以选择列中与选定的解码器开关 12_n 相连的任何列。

图 4 显示了用于行解码开关 15_n 的选择逻辑真值表 40，它与真值表 30 的列选择类似。通过把逻辑高电平信号加到有关的数据输入线 R_n 上，可以选择特定的行解码开关 15_n。在选定的行解码开关 15_n 中，四行中的一行的

选择，是借助地址线 B_0、 $\overline{B_0}$、 B_1和 $\overline{B_1}$而进行的。 输出 R_0借助可编程电流吸收器而与一个电流陷落相电连接，且当得到连接时指定了逻辑电路中的1。当地址信号输入 B_0处于高电平（在真值表 40 中被指定为 1）时，来自地址线的输入的变化确定了与解码器开关 15_n 相连的哪一个行将得到激活。如结合图 3 的真值表 30 所描述的，真值表 40 的四行 41 至 44 显示了选择与具体的解码器开关 15_n有关的阵列 10 的四行的选择所需的逻辑。

参见图 5，其中示意显示了解码开关 122 的一个单个的列电路 50。如将更详细地描述的，各个列解码开关 12 都包括四个列电路 50。列电路 50 包括串联在可编程电源 54 与阵列 11 的一个具体的列之间的两个场效应晶体管（FET）52 和 53。在该具体实施例中，可编程电源 54 与作为数据信号 C_n的选定列解码开关 12 的输入端相耦合。在该具体列电路中，地址线 A_0与 FET 52 的栅极相连。当逻辑高电平出现在地址线 A_0上时，FET 52 把由可编程电源 54 提供的一个 5 伏特电势，耦合到第二个 FET 53。当寻址信号 A_0处于逻辑低电平时，FET 52 不 把该 5 伏特电势耦合到 FET 53。

地址线 A_1通过两个电平移动二极管 55 和 56 而与 FET 53 的栅极相连，而电平移动二极管 55 和 56 与地址线 A_1串联。电平移动二极管 55 和 56 向 FET 53 的栅极提供了电压移动，以防止 FET 53 的栅极—漏极二极管的正向偏置。借助 MESFET 电路，电平移动二极管 55 和 56 被用来防止 MESFET 栅极被驱动成正向偏置。如所示，场效应晶体管 53 当地址线 A_1处于高电平时导通并将来自 FET 52 的 5 伏特电势耦合到阵列 11 的相应的列（被 显示为终端 57）。地址线 A_1上的逻辑低电平阻止了 FET 28 的导通。

参见图 6，一个行电路 60 得到了示意显示，四个这样的电路构成了一个完整的行解码开关 15。行电路 60 包括串联在阵列 11 的相应的行与电流陷落 64 之间的两个 FET 62 和 63，而电流陷落 64 是前述的可编程电陷落。在此具体实施例中，可编程电陷落 64 与作为数据信号 R_n的选定行解码开关 15 的输入端相耦合。当地址线 B_0把逻辑高电平信号加到栅极上时，FET 62 将阵列 11 的相应的行耦合到 FET 63。地址线 B_1必须处于逻辑高电平，才能激活 FET 63 以完成至电流陷落 64 的电路。电流陷落 64 当逻辑高电平信号被加到数据线 R_n（在图 6 中被显示为一个终端）上 时被电耦合到

FET63。电流陷落 64 必须得到电连接，以使电流能够通过行电路 60 流动。从阵列 11 的相应的行至电流陷落 64 的导电性，完成了激活具体寻址的 LED 以使其发光的电路（假定至少一个列电路 50 得到了激活）。

参见图 7，LED 阵列集成电路 10 得到了示意显示。其某些部分被除去了。集成电路 10 包括在 LED 矩阵 11 中的多个 LED。作为一个例子，具体的 LED 70 的一个终端被电连接到第一个列解码开关 12（在图中为了方便而用虚线包围起来）的第一个列电路 50（在图 5 中得到单独显示）。LED 70 的第二终端与行解码开关 15（为了方便而用虚线包围起来）中的一个第一行电路 60（在图 6 中得到单独显示）相连，以作为对用来激活 LED 阵列 11 的多个列和行的多个列解码开关和多个行解码开关的个别显示。该图显示了图 2 的四个 LED 电路装置，其中一个列解码开关 12 通过把可编程电源 54 连接到所寻址的列而激活四个列，而相应的行解码开关 15 通过将被寻址的行从四个行解码开关 15 电连接到电流陷落 62，而完成了该电路。列电路 50 通过可编程电源 54（被显示为块 72）中的一个电路或开关，而与数据线 C_0 上的可编程电源 54 相连，或者以其他方式完成至可编程电源 54 的电路。类似地，行电路 60 通过可编程电流陷落 64（显示为块 74）中的一个开关或电路，而与数据信号 R_0 上的可编程电流陷落 64 相连，或者以其他方式完成至电流陷落 64 的电路。

应该理解的是，可编程电源 54 和可编程电流陷落 64，除了在任何预定的时间所提供的功率量是可编程的之外，还可以得到编程，以通过数据线 C_0 至 C_{58} 上的输入信号的预定程序和在数据线 R_0 至 R_{35} 上的输入信号的预定程序自动地进行排序。

图 8 所示的是低功率解码开关 82（显示为单个的 FET）和 LED 阵列 83（显示为单个的 LED）单片集成在同一基底上的外延结构 80。LED 阵列 83 包括多个依次形成在半绝缘砷化镓基底 84 上的掺杂和未掺杂外延层。如所示，这些外延层是 n+-GaAs 层 85、n-InGap 层 86、n-AlInP 层 87、未掺杂的 AlGaInP 层 88、未掺杂的 AlInP 层 89、P - AlInP 层 90、大约 200Å 厚的 P - InGaP 层 91、以及大约 500Å 厚的未掺杂 GaAs 层 92，以形成与相应的开关 82 相集成的 LED 阵列 83。显示的还有为象素绝缘而

设置的插入片 94、为至每一个象素的较低端的电连接而提供的插入片 95、和为行绝缘而提供的插入片 96。借助触头 97 和 98，提供了至阵列 83 中的每一个 LED 的金属化连接。开关 82 包括器件绝缘插入片 100、源极和漏极连接插入片 102 和 104、以及分别用于源极、栅极和漏极的金属化触头 112、113 和 114。在 1995 年 9 月 26 日颁发的、题目为“插入 LED 阵列的制造方法”并转让给同一受让人的美国专利第 5，453，386 号中，可以找到有关这种阵列的其他信息。另外，关于集成技术，参见 1996 年 1 月 9 日颁发的、题目为“带有二极管解码器的电-光集成电路”并转让给同一受让人的美国专利第 5，483，085 号。

图 9 中显示了一种修正的外延结构 120，它包括以单片集成的方式与 LED 阵列 130 集成在同一基底上的解码开关 122。LED 阵列 130 与图 8 的 LED 阵列 83 类似。解码开关 122 与图 8 的开关 82 类似，只是它是通过在器件制造期间把在 LED 阵列 130 上额外的外延层从 LED 130 添加至 FET 122 而制成的，从而使 p 掺杂物的扩散较为容易。

因此，公布了用更为简单和少的数据驱动器和更少的 I/O 终端来制造显示器特别是彩色显示器的方法。还公布了利用数字数据驱动器的新颖的改进的发光器件驱动矩阵，且特别是利用较少的数据驱动器的发光器件矩阵。另外，还公布了所用功率比相应的现有技术显示器小得多且更为便宜、更小且更容易制造的矩阵显示器和驱动器电路。本发明提供了一种 LED 显示器，它将用于列和行选择的解码开关集成在单片集成阵列中，且 LED 矩阵中用于列和行选择的 I/O 终端数目减小了很多。当然还应该理解的是，可以只用一个列或行解码开关组件来提供 LED 显示器，而其他的行或列解码开关组件（这些当然是可互换的）可以用正常的硬件连接、某种形式的解码、移位寄存器等等来取代。

借助可编程电源和可编程电流陷落，用于解码开关的器件的数目能够减到最小。功率消耗通过驱动器漏电流而不是 MESFET 漏电流而得到限制。其结果，功率消耗比采用不带可编程电源或可编程电流陷落的阵列所获得的要低得多。

所有列解码开关都具有公共地址线。其结果，列可以以 n/4 的方式得

到依次扫描，其中 n 是一次的列数并取决于来自驱动器的输入功率。所有的行解码开关都具有公共地址线。其结果行可以依次或以 m/4 的方式得到扫描，其中 m 是一次的行数并取决于可编程电流陷落的状态。用于防止 MESFET 栅极被驱动到正向偏置状态的电平移动二极管，　　被置于一个 CMOS 驱动器上，以提供解码开关序列扫描。

本发明减小了激活 LED 象素的 I/O 终端的数目，并大大降低了 LED 集成电路的功率消耗。通过将低功率解码开关与 LED 阵列单片集成在同一基底上，功率得到了大大降低。例如，在传统的解码器中，用于 240 乘 140LED 阵列的功率为 11 瓦，而本发明的解码开关 LED 阵列的只有 36 毫瓦。I/O 终端的减少—从 384 至 140 个—大大地改进了 LED 阵列，而不用集成解码开关。

对在此为了说明的目的而选择的实施例的各种修正和改变，对于本领域的技术人员来说是显而易见的。例如，集成电路可以用任何方便的半导体材料系统或任何方便的有机系统制成。另外，LED 阵列和开关能够以各种方式制成，而仍然能够执行所述的功能。另外，可以采用各种不同的发光器件，且这些器件可以用在一定程度上修正和/或互换的步骤来制成。

以上只是以举例的方式进行了描述。在不脱离如权利要求书所述的本发明的范围的前提下，本领域的技术人员可以作出各种其他修正和改变。

以上已经以明确而简明的方式充分描述和公布了本发明及其最佳实施例，从而使本领域的技术人员能够理解并实施本发明及其最佳实施例。

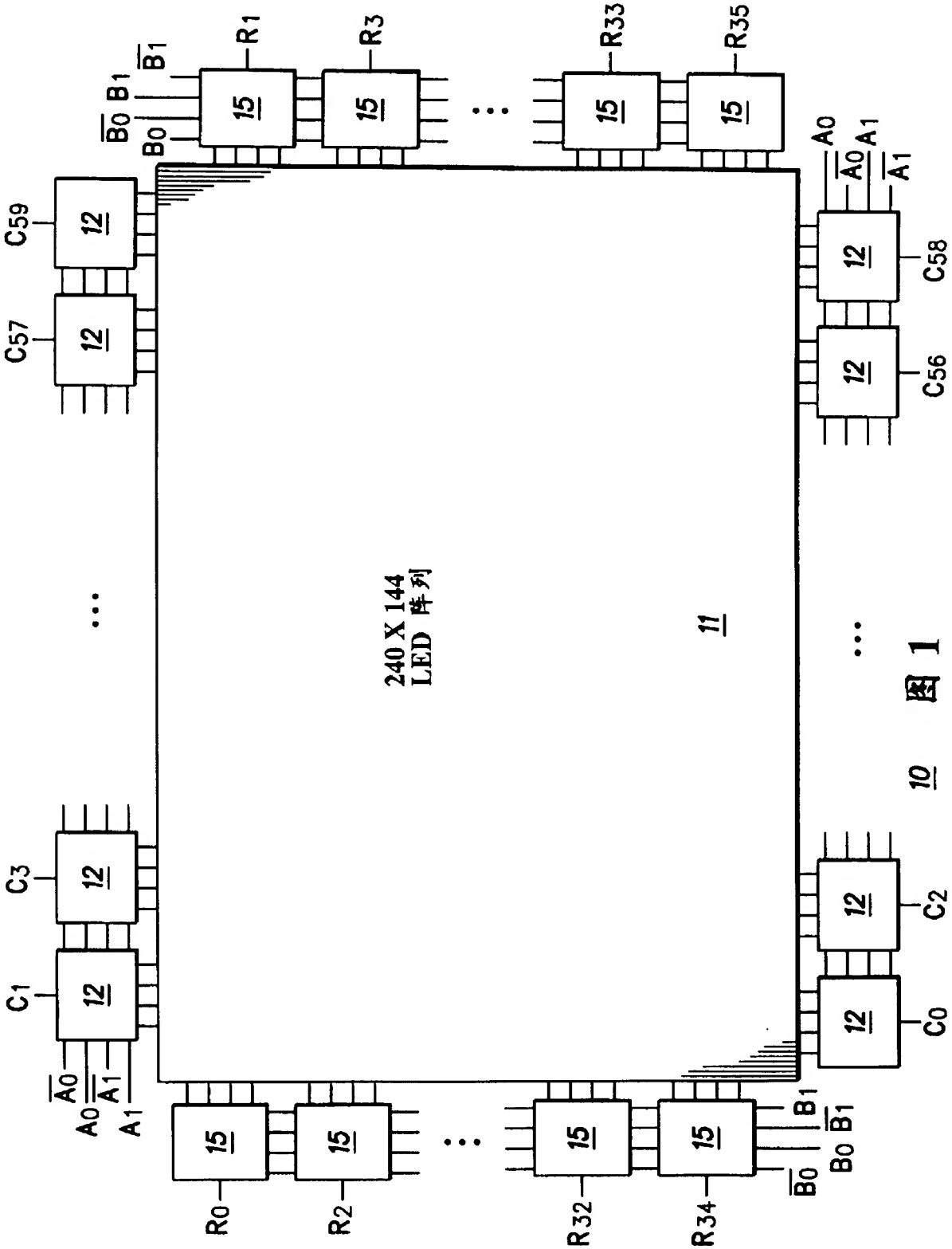

240 X 144
LED 阵列
11
10
R0
R1
R2
R3
R32
R33
R34
R35
C0
C1
C2
C3
C56
C57
C58
C59
A0
A1
B0
B1
12
15

图 1

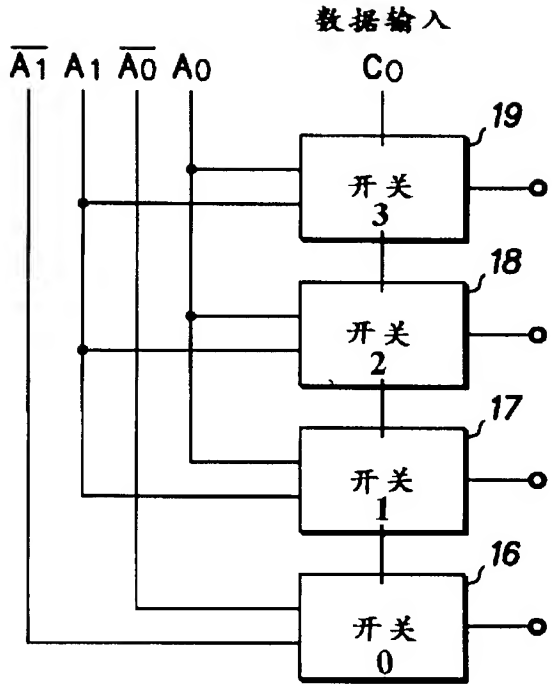


图 2

12

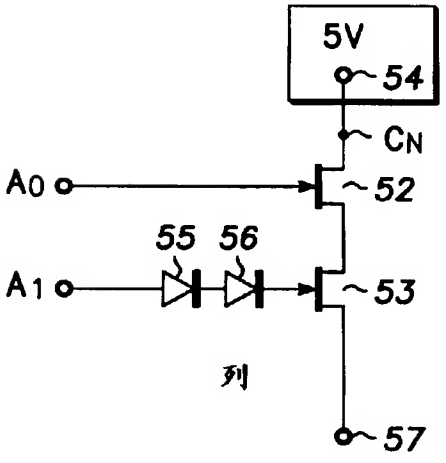
C_N	A_0	$\overline{A_0}$	A_1	$\overline{A_1}$	所选列	
1	0	1	0	1	0	31
1	0	1	1	0	1	32
1	1	0	0	1	2	33
1	1	0	1	0	3	34

图 3

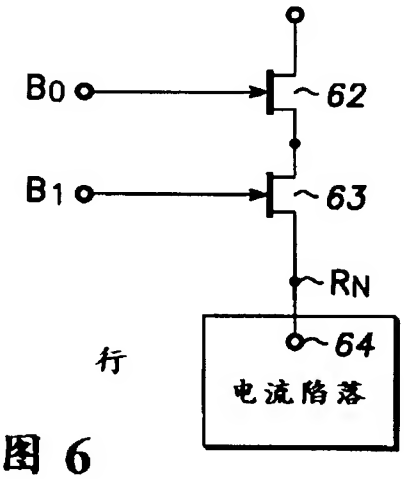
30

R_N	B_0	$\overline{B_0}$	B_1	$\overline{B_1}$	所选行	
1	0	1	0	1	0	41
1	0	1	1	0	1	42
1	1	0	0	1	2	43
1	1	0	1	0	3	44

40 图 4



50 图 5



60 图 6

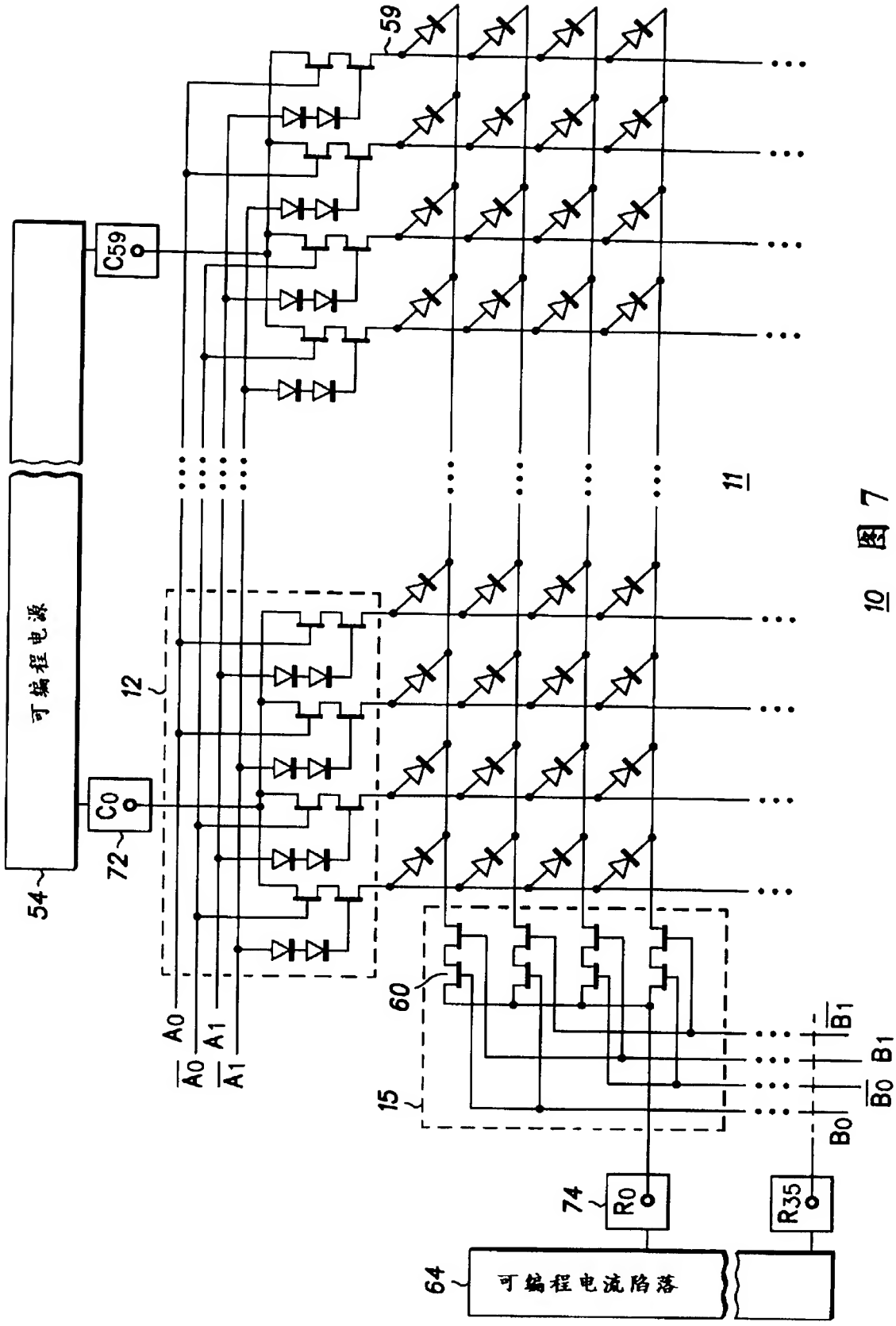

可编程电源
可编程电流陷落
C59
C0
R0
R35
59
54
72
74
64
12
11
10
15
60
A0
$\overline{A0}$
A1
$\overline{A1}$
B0
$\overline{B0}$
B1
$\overline{B1}$

图 7

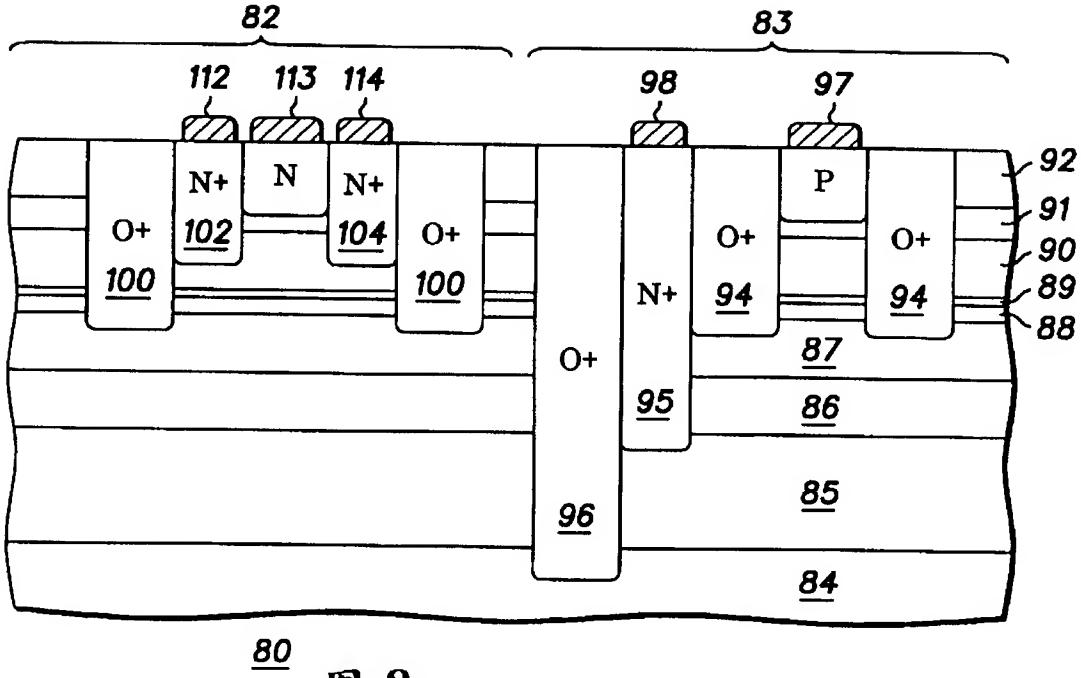

82
83
112
113
114
98
97
92
91
90
89
88
N+
N
N+
P
O+
102
104
O+
O+
O+
100
100
94
94
N+
O+
87
95
86
85
96
84
80

图 8

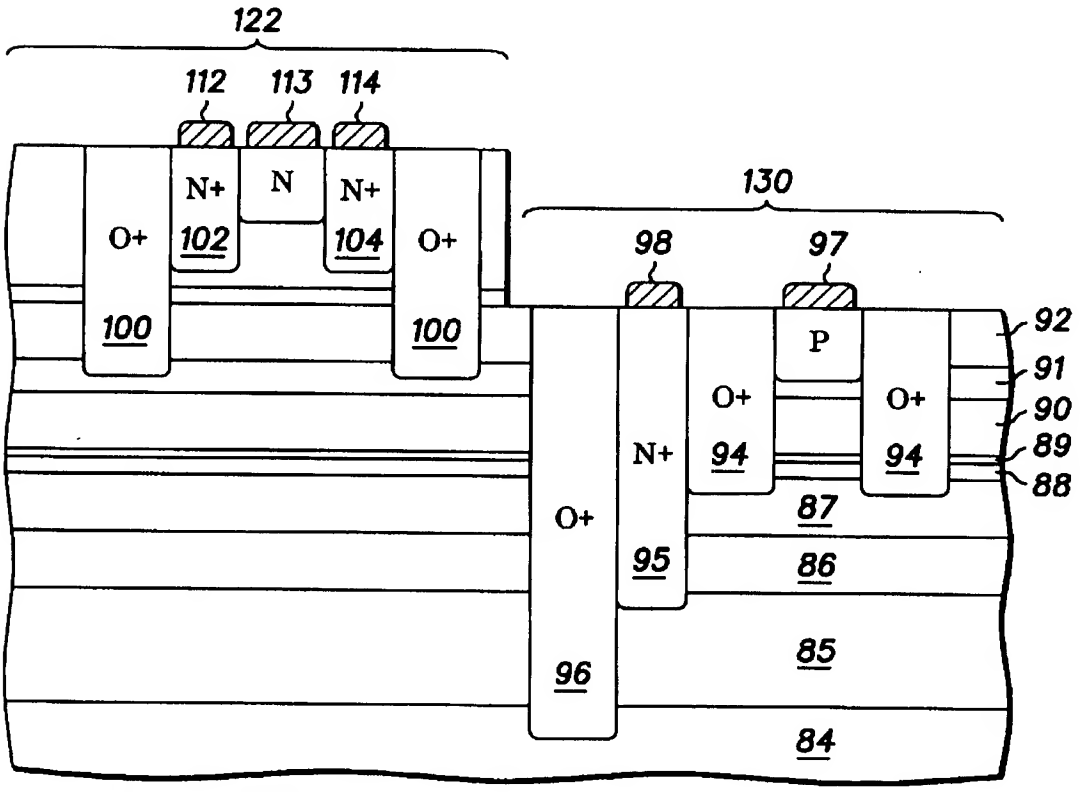

122
112
113
114
130
98
97
92
91
90
89
88
N+
N
N+
P
O+
102
104
O+
O+
O+
100
100
94
94
N+
87
95
86
O+
85
96
84
120

图 9